

IEEE1394 AND IECG1883 PACKET FORMATS

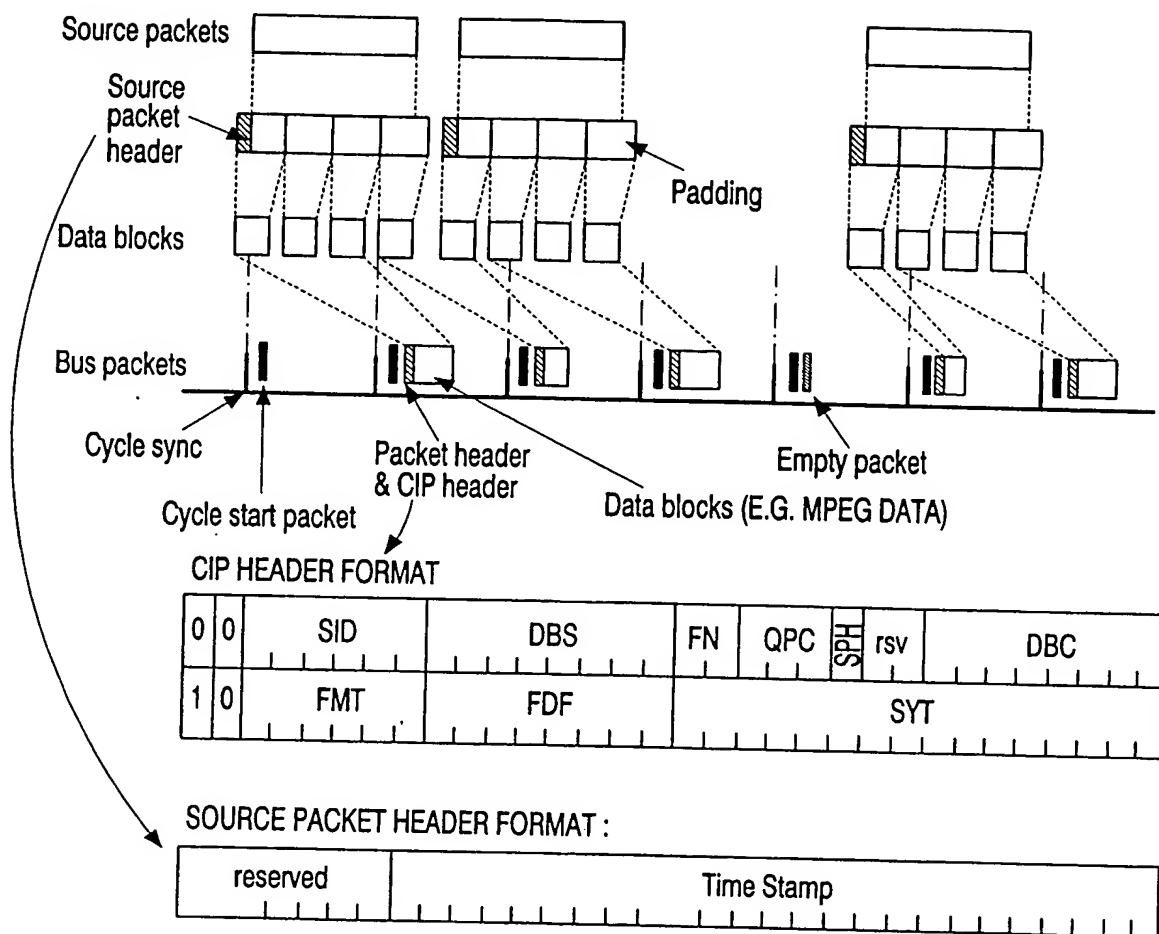


FIG. 1

CYCLE TIME REGISTER FORMAT

second_count	cycle_count	cycle_offset
7	13	12

FIG. 2

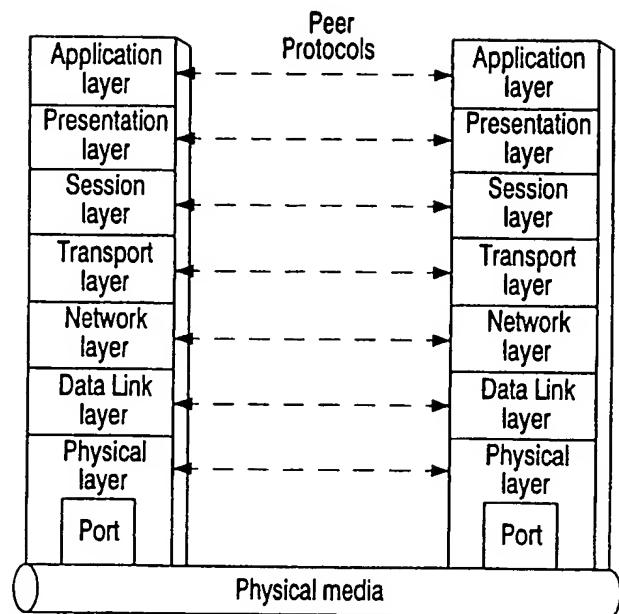


FIG. 3

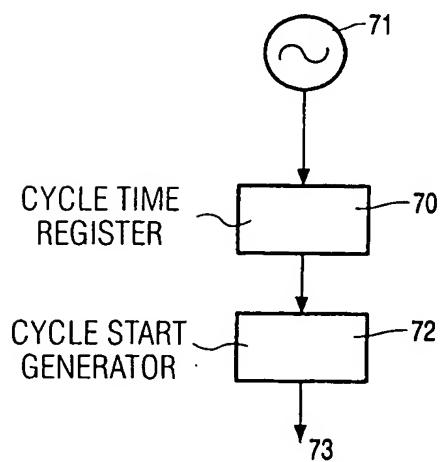


FIG. 7

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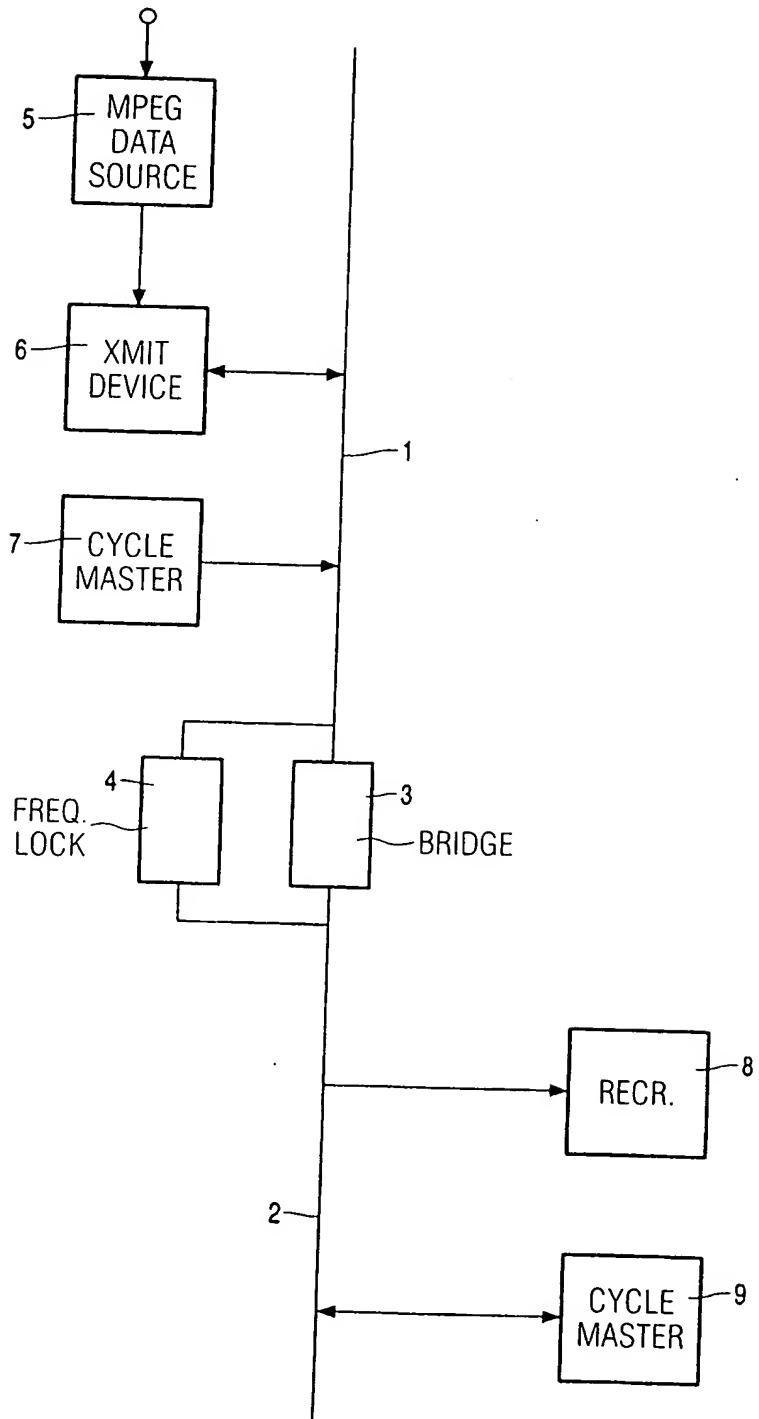


FIG. 4

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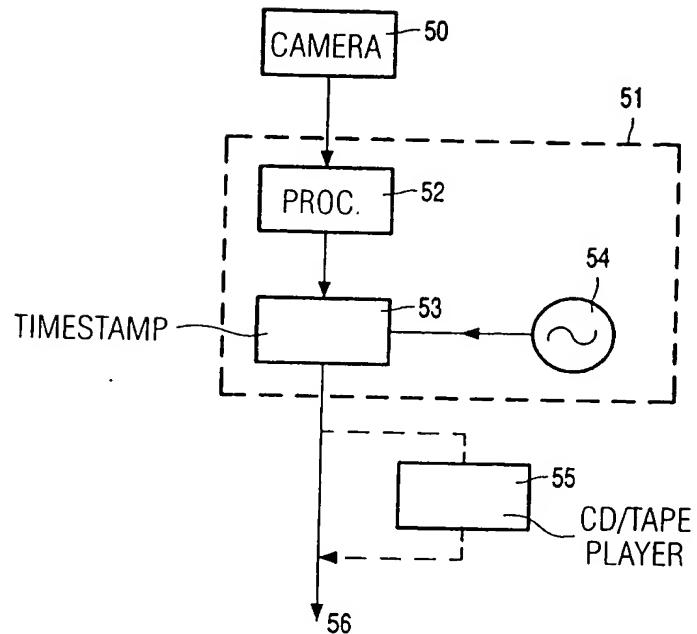


FIG. 5

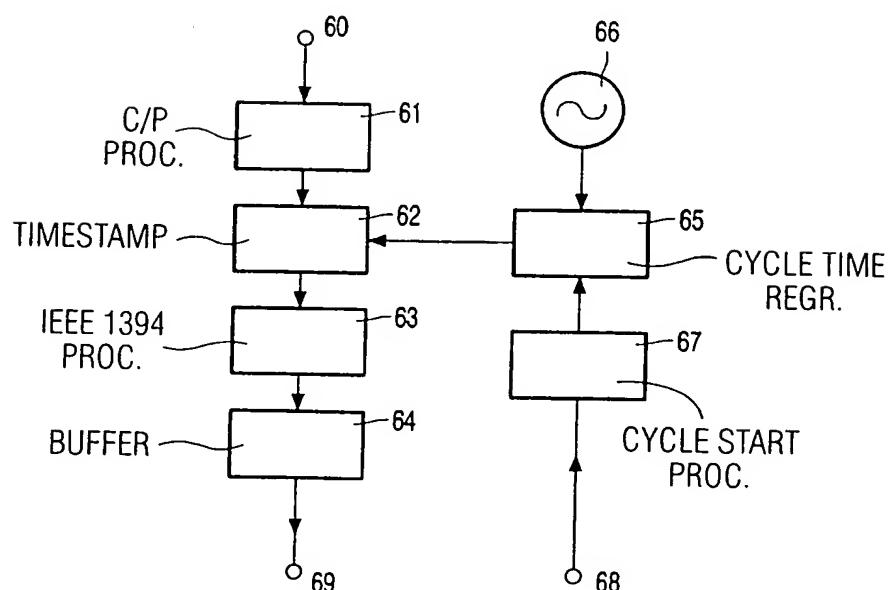


FIG. 6

FIG. 8

24.576MHz Clock [10]

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